IN THE CLAIMS:

1. A signal processing apparatus, comprising:
a channel pooling signal processor, including:
a plurality of computation units;
a test interface for testing the function of said plurality of computation units;
a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and
an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and
a digital signal processor connected to said channel pooling signal processor;
wherein said channel pooling signal processor performs more computationally intensive signal processing operations and said digital signal processor performs less computationally intensive signal processing operations.

2. The signal processing apparatus of Claim 1, wherein a computation unit of said plurality of computation units comprises:
a data sequencer for controlling program execution;
a configurable logic unit; and
a dedicated memory.

3. The signal processing apparatus of Claim 1, further comprising:
a second channel pooling signal processor for processing multiple data streams of voice and data information.

4. The signal processing apparatus of Claim 1, wherein said plurality of computation units are heterogenous computation units.

5. The signal processing apparatus of Claim 1, wherein said plurality of computation units are homogeneous computation units.

6. A method for signal processing, comprising the steps of:
processing high complexity algorithms in a channel pooling signal processor, said channel pooling signal processor including:
a plurality of computation units;
a test interface for testing the function of said plurality of computation units;

a general purpose microprocessor for managing data flow into and out of said channel pooling signal processor; and

an interconnect mechanism for connecting said plurality of computation units, said test interface, and said general purpose microprocessor; and

processing low complexity algorithms in a digital signal processor connected to said channel pooling signal processor.

7. The method of Claim 6, further comprising the steps of:

controlling program execution in a computation unit of said plurality of computation units;

configuring a configurable logic unit in said computation unit in accordance with a standard; and

storing program execution instructions in a dedicated memory in said computation unit.

8. The method of Claim 6, further comprising the steps of:

processing multiple data streams of voice and data information in a second channel pooling signal processor.